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S205D-M Beidou-3 Short Message Communication Chip

specification

V1. 2-20241213

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Catalogue

1. Product Introduction

Figure 1 Product Appearance Diagram

The S205D-M Beidou-3 Short Message Communication Chip (S205D-M) supports both Beidou-3 regional short message communication and Beidou-2 RDSS (Radio Data Service System) functions. Featuring a highly integrated design, it combines anti-interference capabilities, low power consumption, and miniaturization. With minimal peripheral components and a compact carrier board area, the chip delivers full RDSS communication functionality, reducing system design complexity, shortening development cycles, and lowering hardware costs for users.

The S205D-M is widely applicable to wearable, portable, and handheld devices, serving critical sectors including emergency response, life-saving operations, power systems, and transportation.

2. Product Features

- The high-integration design of the RF baseband in the RDSS system;
- The system integrates high-capacity, low-power dynamic random access memory (DRAM, 32 MB) and non-volatile memory (NVM, 8 MB) within the same device.
- Supports both BeiDou-2 short message and BeiDou-3 regional short message communication, with a maximum length of 1000 Chinese characters.
- Supports 800MHz main frequency and high-performance floating-point operations.
- 10mm×10mm small package.

3. Encapsulation Size

The device is packaged in a plastic BGA 256 pin package. The pin center-to-center distance is 0.60 mm, with a ball diameter of 0.30 mm. The package dimensions are 10 mm (length) × 10 mm (width) × 1.52 mm (height). The external dimensions are shown in Figure 2.

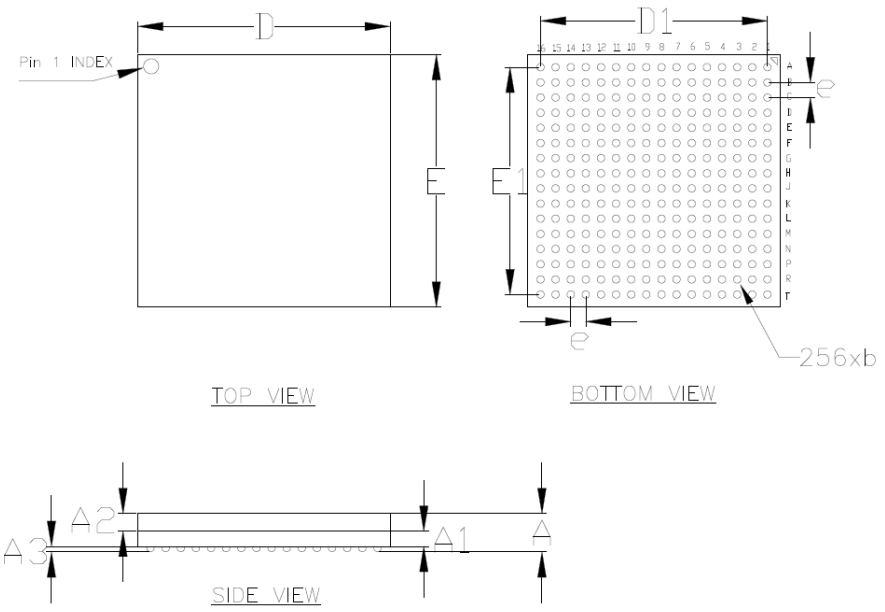

Figure 2 Device外形 Dimensions Diagram

Dimensional tolerances are shown in Table 1.

Table 1 Device Package Dimension Tolerance Table

Dimension Symbol	Dimension value (unit: mm)		
	Minimum	Nominal	Maximum
A	1.36	1.52	1.68
A1	0.54	0.60	0.66
A2	0.65	0.70	0.75
A3	0.17	0.22	0.27
D	9.9	10.0	10.1
E	9.9	10.0	10.1
D1	8.95	9.00	9.05
E1	8.95	9.00	9.05
e	0.60		
b	0.25	0.30	0.35

4. Qualification

Table 2 Key Performance Indicators

Performance index		
RDSS function	Receiving frequency	Receive exit signals S1I and S2C, operating within the frequency range of 2491.75 MHz ± 8.16 MHz.
	Receiving sensitivity	S1I: Bit error rate ≤1×10^{-5} at signal power of-127.6dBm

Performance index		
		S2C:24kbps information frame, bit error rate: ≤1×10^{-5}(signal power-123.8dBm)
		S2C:16kbps information frame, bit error rate: ≤1×10^{-5}(signal power-127.5dBm)
		S2C:8kbps information frame, bit error rate: ≤1×10^{-5}(signal power-130dBm)
	Number of receiving beams	Beidou-2: 10; Beidou-3: 14
	Transmit frequency	Lf0 ： 1615.68 MHz±4.08MHz
		Lf1 ： 1614.26 MHz±4.08MHz
		Lf2 ： 1618.34 MHz±4.08MHz
	Transmitting power	-10dBm to +10dBm (typical value: 2dBm)
	Frequency accuracy of transmission	≤5×10^{-7}
	Modulation phase error of transmitting signal	≤3°
	Short message communication capacity	The maximum length of a single BeiDou-2 message is 120 Chinese characters.
		The maximum length of BeiDou-3 regional messages is 1000 Chinese characters.
Service voltage		Core: 0.83V IO：1.2V、1.8V、3.3V
Power dissipation		≤500mW
Physical characteristics		
Structure size		10mm×10mm
Encapsulation form		BGA 256
Environment pointer		
Working temperature		-40℃~+85℃
Storage temperature		-55℃~+125℃
Certification status		
Certification status		ROHS certification
		REACH certification
Chip interface		
Functional interface		UART, I^2C, PPS, SPI, GPIO, ODO, etc.
Note: The final application performance is subject to the actual firmware loaded.		

5. Pin Definition

Table 3 Device Package Pin Names and Descriptions

Pin number	Pin name	Pin type	Pin function description
D12、E13、G13、H14	+1.2V_VDDRQ	Power input	DDR 1.2V power supply
G14	+1.8V_VDDR	Power input	DDR 1.8V power supply
P2	1625X_3V3_TX_PA	Power input	RF transmit power supply port, DC voltage 3.3V or 1.8V
P5、R6	1625X_VBAT	Power input	RF power port, DC voltage 3.3V or 1.8V
N5、N6	1625X_VDD_IO	Power input	RF power port, DC voltage 3.3V
D6	ADC_AVDD	Power input	ADC 0.8V Analog Power Supply

Pin number	Pin name	Pin type	Pin function description
D4	ADC_AVDDIO	Power input	ADC IO 1.8V power supply
D8	ADC_DVDD	Power input	ADC 0.8V Digital Power Supply
H3	AVDD33_LDO	Power input	RTC LDO 3.3V Input
F8	PLL_AON_AVDD	Power input	PLL 1.8V Analog Power Supply
G7、H8	PLL_AVDD	Power input	PLL 1.8V Analog Power Supply
G2	PVDD_IF	Power input	1.8V intermediate frequency IO power supply
G3	PVDD18_32K	Power input	OSC32K 1.8V power supply
F10	PVDD18_AON	Power input	1.8V IO power supply
K3	PVDD18_BL	Power input	1.8V IO power supply
G12	PVDD18_Q0	Power input	1.8V IO power supply
B2	PVDD18_RNRD	Power input	1.8V clock power supply
F2	PVDD33_32K	Power input	OSC32K 3.3V power supply
G10	PVDD33_AON	Power input	3.3V IO power supply
K2	PVDD33_BL	Power input	3.3V IO power supply
G11	PVDD33_Q0	Power input	3.3V IO power supply
B1	PVDD33_RNRD	Power input	3.3V clock power supply
J16	VCC_FLASH	Power input	Non-volatile memory power supply 3.3V
F9	VDD_AON	Power input	0.8V core logic power supply
D10、E11、F12、G9、H10、H12	VDD_CORE	Power input	0.8V core logic power supply
E7、E9、F6	VDD_NAE	Power input	0.8V core logic power supply
C5、E3、E5、F4	VDD_RDRX	Power input	0.8V core logic power supply
H2	VDD_RTC	Power input	RTC logic power supply 0.8V
G5、H4、H6	VDD_TE	Power input	0.8V core logic power supply
E2	AVDD08_LDO	Power output	RTCLDO0.8V output
F3	AVDD18_LDO	Power output	RTCLDO1.8V output
L1、L2、L3、L4、L5、L6、L7、L16、M5、M7、M10、M11、M12、N8、N10、N13、P1、P8、R2、R4、R9、R13、R15、T1、T3、T5、T9、T12、T14、T16	RF_GND	Reference site	RF reference ground

Pin number	Pin name	Pin type	Pin function description
C4、C6、D5、D7、D9、D11、D13、E4、E6、E8、E10、E12、E14、F5、F7、F11、F13、G4、G6、G8、H5、H7、H9、H11、H13	VSS	Reference site	Digital signal reference ground
N1	1625X_IF_N(MAG0)	O	Analog Intermediate Frequency Differential Output of Radio Frequency Circuit of Radio Data System
M1	1625X_IF_P(MAG1)	O	Analog Intermediate Frequency Differential Output of Radio Frequency Circuit of Radio Data System
M6	1625X_SYS_CLK	O	RF circuit reference clock
T2	1625X_TX_OUT	O	Radio frequency transmission channel output
C9	BP_ZQ	O	ZQ calibration, 240 ohm 1% resistance for ground connection
F14	LPDDR2_ZQ	O	ZQ calibration, 240 ohm 1% resistance for ground connection
L13	SIM_RST	O	SIM card reset
E1	XO	O	RTC crystal oscillator output
N4	1625X_SPI_SCLK	I/O	RF circuit SPI clock
N3	1625X_SPI_SDIO	I/O	RF circuit SPI data
M4	1625X_SPI_SS	I/O	Radio Frequency Circuit SPI Chip Select
K13	IRIGB_MARK/GPIO_C27	I/O	B code interface flag/GPIO
K16	IRIGB_O/GPIO_C25	I/O	B code interface output/GPIO
K15	IRIGB_PPS_OUT/GPIO_C26	I/O	B code interface PPS/GPIO
L10	BPSK/GPIO_D26	I/O	RDSSTX output /GPIO
H15	CLK_5M/GPIO_D17	I/O	Configurable clock output/GPIO
K11	EXT_LAT0/GPIO_D24	I/O	External latch-in/gpio
D2	GPIO_D_27	I/O	GPIO
D3	GPIO_D_28	I/O	GPIO
C3	GPIO_D_29	I/O	GPIO
C2	GPIO_D_30	I/O	GPIO
J1	GPIO0/UART3_RXD	I/O	GPIO/UART3 RX with interrupt capability
J2	GPIO1/UART3_TXD	I/O	GPIO/UART3 TX with interrupt capability
H1	GPIO2/UART6_RXD	I/O	Interrupt-enabled GPIO/UART6 RX
K4	GPIO3/UART6_TXD	I/O	GPIO/UART6 TX with interrupt capability
F1	GPIO4/UART6_CTS	I/O	GPIO/UART6 CTS with interrupt capability
G1	GPIO5/UART6_RTS	I/O	Interrupt-enabled GPIO/UART6 RTS

Pin number	Pin name	Pin type	Pin function description
J3	GPIO6/UART7_RXD	I/O	GPIO/UART7 RX with interrupt capability
K1	GPIO7/UART7_TXD	I/O	GPIO/UART7 TX with interrupt capability
L11	I2C0_SCL/GPIO_A24	I/O	I2C0 clock/GPIO with interrupt capability
L12	I2C0_SDA/GPIO_A25	I/O	I2C0 data/GPIO with interrupt capability
K14	IRIGB_I/GPIO_C28	I/O	B code interface input/GPIO
G15	ODO_DIR/GPIO_C24	I/O	Gauge direction input/GPIO
H16	ODO_PULSE/GPIO_C23	I/O	Gauge Pulse Input/GPIO
K12	PPS0/GPIO_D22	I/O	Second Pulse Output/GPIO
L15	SIM_CLK/GPIO_A28	I/O	SIM card clock / GPIO with interrupt capability
L14	SIM_IO/GPIO_A29	I/O	SIM card data/GPIO with interrupt capability
J6	SPI0_CLK/GPIO_A30	I/O	SPI Master Controller 0 Clock/ Interrupt-enabled GPIO
J4	SPI0_CSN0/GPIO_A31	I/O	SPI main controller 0 chip select 0/ GPIO with interrupt capability
J7	SPI0_MISO/GPIO_B0	I/O	SPI Master Controller 0 Data Input/GPIO
J5	SPI0_MOSI/GPIO_B1	I/O	SPI Master Controller 0 Data Output/GPIO
K5	SPI1_CLK/GPIO_B2	I/O	SPI Master Controller 1 Clock/GPIO
K6	SPI1_CSN0/GPIO_B3	I/O	SPI Master Controller 1 Pin Select 0/GPIO
K7	SPI1_MISO/GPIO_B5	I/O	SPI Main Controller 1 Data Input/GPIO
L8	SPI1_MOSI/GPIO_B6	I/O	SPI Main Controller 1 Data Output/GPIO
J13	UART0_RXD/GPIO_B27	I/O	Serial port UART0 RX, boot loader serial port/GPIO
J12	UART0_TXD/GPIO_B26	I/O	Serial port UART0 TX, boot loader serial port/GPIO
J14	UART1_RXD/GPIO_B29	I/O	Serial port UART1 RX/GPIO
J15	UART1_TXD/GPIO_B28	I/O	Serial port UART1 TX/GPIO
J11	UART2_RXD/GPIO_B31	I/O	Serial port UART2 RX/GPIO
J10	UART2_TXD/GPIO_B30	I/O	Serial port UART2 TX/GPIO
R1	1625X_BPSK	I	BPSK signal input for RF transmission channel
T7	1625X_CHIP_EN	I	The RF circuit activates when the signal is either suspended or at a high voltage level. Turn off at low level
T4	1625X_RF_IN	I	RF input terminal of receiving channel
R7	1625X_RSTN	I	Set to high level for internal reset, or connect to external reset signal

Pin number	Pin name	Pin type	Pin function description
T8	1625X_RX_EN	I	The high-level RF receive channel is enabled, and the low-level receive channel is disabled.
M3	1625X_TCXO	I	TCXO signal input port
R3	1625X_TX_EN	I	Enable the RF transmit channel. The suspended or high-level transmit channel is active, while the low-level transmit channel is inactive.
B4	IF_AIN_I0_N	I	Baseband ADC CH0 I-channel analog input N terminal
A4	IF_AIN_I0_P	I	Baseband ADC CH0 I-channel analog input P terminal
B6	IF_AIN_I1_N	I	Baseband ADC CH1 I-channel analog input N terminal
A6	IF_AIN_I1_P	I	Baseband ADC CH1 I-channel analog input P terminal
B8	IF_AIN_I2_N	I	Baseband ADC CH2 I-channel analog input N terminal
A8	IF_AIN_I2_P	I	Baseband ADC CH2 I-channel analog input P terminal
B10	IF_AIN_I3_N	I	Baseband ADC CH3 I analog input N terminal
A10	IF_AIN_I3_P	I	Baseband ADC CH3 I analog input P terminal
B3	IF_AIN_Q0_N	I	Baseband ADC CH0 Q-channel analog input N terminal
A3	IF_AIN_Q0_P	I	Baseband ADC CH0 Q-channel analog input P terminal
B5	IF_AIN_Q1_N	I	Baseband ADC CH1 Q-channel analog input N terminal
A5	IF_AIN_Q1_P	I	Baseband ADC CH1 Q-channel analog input P terminal
B7	IF_AIN_Q2_N	I	Baseband ADC CH2 Q-channel analog input N terminal
A7	IF_AIN_Q2_P	I	Baseband ADC CH2 Q-channel analog input P terminal
B9	IF_AIN_Q3_N	I	Baseband ADC CH3 Q-channel analog input N terminal
A9	IF_AIN_Q3_P	I	Baseband ADC CH3 Q-channel analog input P terminal
M9	POWER_OK	I	Reset signal, input low level valid
A1	RD_CLK	I	RDSS sampling clock
A2	RN_CLK	I	RNSS sampling clock
K8	STRAP_0	I	Enable software setting 0
J8	STRAP_1	I	Enable software setting 1
J9	STRAP_2	I	Enable software setting 2
K9	STRAP_3	I	Enable software setting 3
L9	STRAP_4	I	Enable software setting bit 4
K10	SYS_CLK	I	The SOC system reference clock input
M8	SYS_RSTN	I	Configure the pin to pull up to 3.3V on a 10K resistor by default

Pin number	Pin name	Pin type	Pin function description
D1	XI	I	RTC crystal oscillator input
C1	XIN	I	External RTC clock input, grounded with a 1M resistor when not in use
D14	VDDR_VREF	DDR refere-nce voltage	DDR reference voltage, +1.2V_VDDRQ/2
R5	1625X_BYP_1	/	BYPASS capacitor terminal, connect an external 1uF capacitor to ground
T6	1625X_BYP_10	/	BYPASS capacitor terminal, connect an external 1uF capacitor to ground
P4	1625X_BYP_2	/	BYPASS capacitor terminal, connect an external 1uF capacitor to ground
P3	1625X_BYP_3	/	BYPASS capacitor terminal, connect an external 1uF capacitor to ground
N2	1625X_BYP_4	/	BYPASS capacitor terminal, connect an external 1uF capacitor to ground
M2	1625X_BYP_5	/	BYPASS capacitor terminal, connect an external 1uF capacitor to ground
P6	1625X_BYP_6	/	BYPASS capacitor terminal, connect an external 1uF capacitor to ground
N7	1625X_BYP_7	/	BYPASS capacitor terminal, connect an external 1uF capacitor to ground
P7	1625X_BYP_8	/	BYPASS capacitor terminal, connect an external 1uF capacitor to ground
R8	1625X_BYP_9	/	BYPASS capacitor terminal, connect an external 1uF capacitor to ground
C8	AON_GPIO_0	/	Keep function, default NC
C7	AON_GPIO_1	/	Keep function, default NC
G16	JTAG0_TCK	/	Keep function, default NC
F16	JTAG0_TDI	/	Keep function, default NC
E15	JTAG0_TDO	/	Keep function, default NC
E16	JTAG0_TMS	/	Keep function, default NC
F15	JTAG0_TRSTN	/	Keep function, default NC
A11、A12、A13、A14、A15、A16、B11、B12、B13、B14、B15、B16、C10、C11、C12、C13、C14、C15、C16、D15、D16、M13、M14、M15、M16、N9、N11、N12、N14、N15、N16、P9、P10、P11、P12、P13、P14、P15、P16、R10、R11、R12、R14、R16、T10、T11、T13、T15	NC	/	Hang in the air

The mapping of these pins is shown in Figure 3.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	RD_CLK	RN_CLK	IF_AIN_Q0_P	IF_AIN_I0_P	IF_AIN_Q1_P	IF_AIN_I1_P	IF_AIN_Q2_P	IF_AIN_I2_P	IF_AIN_Q3_P	IF_AIN_I3_P	NC	NC	NC	NC	NC	NC
B	PVDD33_RNRD	PVDD18_RNRD	IF_AIN_Q0_N	IF_AIN_I0_N	IF_AIN_Q1_N	IF_AIN_I1_N	IF_AIN_Q2_N	IF_AIN_I2_N	IF_AIN_Q3_N	IF_AIN_I3_N	NC	NC	NC	NC	NC	NC
C	XIN	GPIO_D_30	GPIO_D_29	VSS	VDD_RDRX	VSS	AON_GPIO_1	AON_GPIO_0	BP_ZQ	NC	NC	NC	NC	NC	NC	NC
D	XI	GPIO_D_27	GPIO_D_28	ADC_AVDDIO	VSS	ADC_AVDD	VSS	ADC_DVDD	VSS	VDD_CORE	VSS	+1.2V_VDDRQ	VSS	VDDR_VREF	NC	NC
E	XO	AVDD08_LDO	VDD_RDRX	VSS	VDD_RDRX	VSS	VDD_NAE	VSS	VDD_NAE	VSS	VDD_CORE	VSS	+1.2V_VDDRQ	VSS	JTAG0_TDO	JTAG0_TMS
F	GPIO 4	PVDD33_32K	AVDD18_LDO	VDD_RDRX	VSS	VDD_NAE	VSS	PLL_AON_AVDD	VDD_AON	PVDD18_AON	VSS	VDD_CORE	VSS	LPDDR2_ZQ	JTAG0_TRSTN	JTAG0_TDI
G	GPIO 5	PVDD_IF	PVDD18_32K	VSS	VDD_TE	VSS	PLL_AVDD	VSS	VDD_CORE	PVDD33_AON	PVDD33_Q0	PVDD18_Q0	+1.2V_VDDRQ	+1.8V_VDDR	ODO_DIR	JTAG0_TCK
H	GPIO 2	VDD_RTC	AVDD33_LDO	VDD_TE	VSS	VDD_TE	VSS	PLL_AVDD	VSS	VDD_CORE	VSS	VDD_CORE	VSS	+1.2V_VDDRQ	CLK_5M	ODO_PULSE
J	GPIO 0	GPIO 1	GPIO 6	SPI0_CSN0	SPI0_MOSI	SPI0_CLK	SPI0_MISO	STRAP_1	STRAP_2	UART2_TXD	UART2_RXD	UART0_TXD	UART0_RXD	UART1_RXD	UART1_TXD	VCC_FLASH
K	GPIO 7	PVDD33_BL	PVDD18_BL	GPIO 3	SPI1_CLK	SPI1_CSN0	SPI1_MISO	STRAP_0	STRAP_3	SYS_CLK	EXT_LAT0	PPS0	IRIG B_MARK	IRIG B_I	IRIG B_PPS_OUT	IRIG B_O
L	RF_GND	RF_GND	RF_GND	RF_GND	RF_GND	RF_GND	RF_GND	SPI1_MOSI	STRAP_4	BPSK	I2C0_SCL	I2C0_SDA	SIM_RST	SIM_IO	SIM_CLK	RF_GND
M	1625X_IP(MAG1)	1625X_BYP_5	1625X_TCXO	1625X_SPI_SS	RF_GND	1625X_SYS_CLK	RF_GND	SYS_RSTN	POWER_OK	RF_GND	RF_GND	RF_GND	NC	NC	NC	NC
N	1625X_IN(MAG0)	1625X_BYP_4	1625X_SPI_SDIO	1625X_SPI_SCLK	1625X_VDD_IO	1625X_VDD_IO	1625X_BYP_7	RF_GND	NC	RF_GND	NC	NC	RF_GND	NC	NC	NC
P	RF_GND	1625X_3V3_TX_PA	1625X_BYP_3	1625X_BYP_2	1625X_VBAT	1625X_BYP_6	1625X_BYP_8	RF_GND	NC	NC	NC	NC	NC	NC	NC	NC
R	1625X_BPSK	RF_GND	1625X_TX_EN	RF_GND	1625X_BYP_1	1625X_VBAT	1625X_RSTN	1625X_BYP_9	RF_GND	NC	NC	NC	RF_GND	NC	RF_GND	NC
T	RF_GND	1625X_TX_OUT	RF_GND	1625X_RF_IN	RF_GND	1625X_BYP_10	1625X_CHIP_EN	1625X_RX_EN	RF_GND	NC	NC	RF_GND	NC	RF_GND	NC	RF_GND

Figure 3 Pin Mapping Diagram

6. Product Label

The product identification is shown in Figure 4.

Figure 4 Product Identification

7. Order Information

Table 4 Order Information Table

Model	Pack
S205D-M	Antistatic vacuum tray packaging, 240 pieces per tray

Revision History Record of Revision

Order number	Documentation Edition	Revision	Date of issue
1	V1.0	Found	2023.12
2	V1.1	Update pin definitions and product identifiers	2024.06
3	V1.2	Add ROHS and REACH documentation	2024.12

Do It Well.

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